IN THE CLAIMS

Please **amend** claims 1 and 18 in accordance with the Status of the Claims, *infra*. Additions are underlined and deletions appear as strikethroughs.

The amendment to claim 18 is not a claim narrowing amendment as that term s understood; but, rather, merely corrects an antecedent basis problem. The amendment to claim 1 is made without surrendering any equivalents to the added subject matter.

SUMMARY OF THE CLAIMS

Claim 1 (currently amended)

1. A memory-integrated display element, comprising:

an optical modulation element provided in a pixel;

a memory element, provided in the pixel, which stores binary data, which indicates a value inputted to the optical modulation element, wherein:

said memory element is arranged by connecting at least an input inverter and and output inverter~~two inverters~~ to each other in a loop manner, wherein

an output of the input inverter is input into the output inverter, and

an output of the~~an~~ output inverter~~, one of the inverters,~~ which functions as an output end of the memory element, is directly connected to one end of the optical modulation element.

Claims 2-17 (original)

2. The memory-integrated display element set forth in claim 1, wherein

said optical modulation element is a current drive type optical modulation element whose luminous intensity varies in accordance with a current quantity.

3. The memory-integrated display element set forth in claim 1, wherein

said optical modulation element is an Organic Light Emission Diode.

4. The memory-integrated display element set forth in claim 1, further comprising

electric charge emitting means for emitting electric charge, which has been stored in the optical modulation element while the memory element was applying a voltage to the optical modulation element, after the memory element finishes applying the voltage.

5. The memory-integrated display element set forth in claim 1, wherein

said output inverter is a complementary inverter.

6. The memory-integrated display element set forth in claim 5, wherein

said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line.

7. The memory-integrated display element set forth in claim 5, wherein

said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line, and

when a ratio of an OFF resistance value of the n type transistor with respect to an ON resistance value of the p type transistor is K,

a ratio of an ON resistance value of the p type transistor with respect to an ON resistance value of the optical modulation element is set to be substantially $(K + 1)^{1/2}/K$.

8. The memory-integrated display element set forth in claim 5, wherein

said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line, and

when a ratio of an OFF resistance value of the n type transistor with respect to an ON resistance value of the p type transistor is K, and a dispersion quantity of lighting luminance of the optical modulation element is within ± x % with respect to a reference value,

a ratio of an ON resistance value of the p type transistor with respect to an ON resistance value of the optical modulation element is set to be a range from $(K + 1)^{1/2} \cdot (1-x/100)/K$ to $(K + 1)^{1/2} \cdot (1 + x/100)/K$.

9. The memory-integrated display element set forth in claim 8, wherein said optical modulation element is a current drive type optical modulation element whose luminous intensity varies in accordance with a current quantity.

10. The memory-integrated display element set forth in claim 8, wherein said optical modulation element is an Organic Light Emission Diode.

11. The memory-integrated display element set forth in claim 5, wherein said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line.

12. The memory-integrated display element set forth in claim 5, wherein said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line, and

when a ratio of an OFF resistance value of the p type transistor with respect to an ON resistance value of the n type transistor is K,

a ratio of an ON resistance value of the n type transistor with respect to an ON resistance value of the optical modulation element is set to be substantially $(K + 1)^{1/2}/K$.

13. The memory-integrated display element set forth in claim 5, wherein said complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line, and

when a ratio of an OFF resistance value of the p type transistor with respect to an ON resistance value of the n type transistor is K, and-a dispersion quantity of lighting luminance of the optical modulation element is within ± x % with respect to a reference value,

a ratio of an ON resistance value of the n type transistor with respect to an ON resistance value of the optical modulation element is set to be a range from $(K + 1)^{1/2} \cdot (1-x/100)/K$ to $(K + 1)^{1/2} \cdot (1 + x/100)/K$.

14. The memory-integrated display element set forth in claim 13, wherein

said optical modulation element is a current drive type optical modulation element whose luminous intensity varies in accordance with a current quantity.

15. The memory-integrated display element set forth in claim 13, wherein

said optical modulation element is an Organic Light Emission Diode.

16. The memory-integrated display element set forth in claim 1, wherein

said optical modulation element and said memory element are included in each of plural sub pixels which make up one pixel unit.

17. The memory-integrated display element set forth in claim 1, wherein

said memory element includes a power electrode which is used also as either of an anode or a cathode of the optical modulation element.

Claim 18 (currently amended)

18. (Amended) The memory-integrated display element set forth in claim 1, wherein

said memory element includes a first power electrode and a second power electrode, and said optical modulation element includes an anode and a cathode, and the first power electrode and the second power electrode are provided separately from the anode and the cathode.

Claim 19 (original)

19. The memory-integrated display element set forth in claim 1, further comprising:

a plurality of data signal lines; and a plurality of select signal lines which cross the data signal lines at right angle, wherein:

said memory element is provided in each of combinations of the data signal lines and the select signal lines, and stores binary data indicated by a data signal line corresponding to the memory element, in a case where a select signal line corresponding to the memory element instructs the memory element to select, and

the memory element is provided adjacent to another memory element, via a reference line, either of the data signal line and the select signal line, so that both memory elements are axially symmetrical with respect to the reference line, and the optical modulation element is provided adjacent to another optical modulation element, via the reference line, so that both optical modulation elements are axially symmetrical with respect to the reference line, and a power line is shared by the both memory elements, or the both optical modulation elements.